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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,146	02/02/2004	Masao Inoue	WILL.0005	6420

7590 08/25/2005

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EXAMINER

TSAI, SHENG JEN

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/768,146

Applicant(s)

INOUE ET AL.

Examiner

Sheng-Jen Tsai

Art Unit

2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>07/01/2005, 02/02/</u> | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. Claims 1-15 are presented for examination in this application (10,768,146) filed on February 2, 2004.

Acknowledgement is made to the Information Disclosure Statement received on February 2, 2004, and July 1, 2005.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites the limitation of **"wherein the maintenance control unit restores the information stored in the control memory, in which the failure has occurred, using a storage area of the control memory storing the first control information."** Note that the failure has occurred in the control memory, as stated in the claim, thus it is questionable how information could be restored using a storage area of the control memory. Either the failed control memory unit has to be replaced with a normal unit and the information is restored in a storage area of the normal control memory unit; or the information is restored using a storage area of a second control memory unit; or else. Applicants need to clarify the intended object of this claim with respect to the control memory unit.

The same issue of claim 4 as described above is also present in claim 11.

Claims 5-10 and claims 12-15 are rejected by virtue of their dependence from claims 4 and 11, respectively.

Therefore, the merits of claims 4-15 have not been evaluated by claim analysis in this Office Action.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Moriwaki et al. (US Patent Application Publication 2004/0083338).

As to claim 1, Moriwaki et al. disclose a **disk array device** [Disk Array Controller (title); figure 1] **comprising plural clusters** [figure 1 shows n clusters], **each of the clusters including:**

Channel adapters which control exchange of data with host apparatuses [channel IF unit, figure 1, 11];

Disk adapters which control exchange of data with storage devices [disk IF unit, figure 1, 12];

Cache memory packages which are mounted with cache memory [cache memory unit, figure 1, 14];

Basic control memory packages which are mounted with basic control memories storing management information concerning a device configuration and a device

operation of disk array device [shared memory unit, figure 1, 13; paragraph 0011];
and

Expanded control memory packages which are mounted with expanded control memory storing directory information concerning a storage structure of the respective cache memory [shared memory, figure 1, 13; with a first memory unit and a second memory unit (paragraphs 0020-0021)] **wherein the management information is multiplexed by the respective basic control memories of the respective cluster and stored therein** [figure 1].

As to claim 2, "refer to As to claim 1." Further, Moriwaki et al. teach that **the first control information** [for storing control information related to the disk array control unit (e.g., information related to the controlling of the data transfer between the channel IF units/disk IF units and the cache memory units) (paragraph 0010)] **and the second control information** [management information of the data to be stored in the disk devices (paragraph 0010)] are stored using a plurality of shared memory units [figure 1; paragraph 0010; with a first memory unit and a second memory unit (paragraphs 0020-0021)].

As to claim 3, Moriwaki et al. teach that **the second control information is storage structure information concerning a storage structure of the respective cache memories** [the control information is related to configuration between the channel IF units/disk IF units and the cache memory units over the plurality of disk array control units (paragraph 0011)].

5. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Minowa et al. (US Patent Application Publication 2003/0221070).

As to claim 1, Minowa et al. disclose **a disk array device** [Storage System (title); figure 1] **comprising plural clusters** [figure 1 shows xn clusters (110 and 130)], **each of the clusters including:**

Channel adapters which control exchange of data with host apparatuses [channel control unit, figure 1, 110];

Disk adapters which control exchange of data with storage devices [disk control unit, figure 1, 130];

Cache memory packages which are mounted with cache memory [cache unit, figure 1, 150];

Basic control memory packages which are mounted with basic control memories storing management information concerning a device configuration and a device operation of disk array device [shared memory unit, figure 1, 140]; and

Expanded control memory packages which are mounted with expanded control memory storing directory information concerning a storage structure of the respective cache memory [shared memory, figure 1, 142] **wherein the management information is multiplexed by the respective basic control memories of the respective cluster and stored therein** [figure 1; abstract].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2186

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dunphy et al. (US 5,077,736), and in view of Belsan (US 5,155,835).

It should be noted that the inventions disclosed by Dunphy et al. and Belsan are assigned to the same assignee (Storage technology Corporation, Louisville, Colorado) and teach different aspects of the same data storage system. Therefore, no further explanation, justification or motivation is considered necessary, and will not be provided by the examiner, for the combination of the two inventions to serve as the ground of the following claim analysis.

As to claim 1, Dunphy et al. and Belsan disclose a **disk array device** [Dunphy et al., Disk Drive Memory (title); Belsan, Multilevel, Hierarchical Dynamically Mapped Data Storage Subsystem (title)] **comprising plural clusters** [Belsan, figure 1 shows two clusters (111 and 112)], **each of the clusters including:**

Channel adapters which control exchange of data with host apparatuses [Dunphy et al., a plurality of channels (figure 1, 151~154 through 130-0~130-M); Belsan, figure 1];

Disk adapters which control exchange of data with storage devices [Dunphy et al., figure 1, the storage control device comprising control modules (101~104); disk drive manager; and directors (151~154); figures 2-4; Belsan, control and device circuits (figure 1, 121) of the disk drive manager (figure 1, 103-1)];

Cache memory packages which are mounted with cache memory [Dunphy et al., figure 2, 203 and figure 3, 305; Belsan, figure 2, 113];

Basic control memory packages which are mounted with basic control memories storing management information concerning a device configuration and a device operation of disk array device [Dunphy et al., figure 4, history log 404; column 9, lines 19-39; column 12, lines 55-68; column 13, lines 1-18]; **and**

Expanded control memory packages which are mounted with expanded control memory storing directory information concerning a storage structure of the respective cache memory [Belsan, a mapping table is easily maintained in memory of this data storage system to indicate which of the logical cylinders contained in the disk drive array (column 2, lines 8-38; figures 8-9) **wherein the management information is multiplexed by the respective basic control memories of the respective cluster and stored therein** [Dunphy et al., figure 1; Belsan, figure 1].

As to claim 2, Dunphy et al. and Belsan disclose **a disk array device** [Dunphy et al., Disk Drive Memory (title); Belsan, Multilevel, Hierarchical Dynamically Mapped Data Storage Subsystem (title)] **comprising plural clusters** [Belsan, figure 1 shows two clusters (111 and 112)], **each of the clusters including:**

Channel adapters which control exchange of data with host apparatuses [Dunphy et al., a plurality of channels (figure 1, 151~154 through 130-0~130-M); Belsan, figure 1];

Disk adapters which control exchange of data with storage devices [Dunphy et al., figure 1, the storage control device comprising control modules (101~104); disk

drive manager; and directors (151~154); figures 2-4; Belsan, control and device circuits (figure 1, 121) of the disk drive manager (figure 1, 103-1));

Cache memory packages which are used by the channel adapters and the disk adapters and have cache memories storing data [Dunphy et al., figure 2, 203 and figure 3, 305; Belsan, figure 2, 113]; and

Plural control memory packages which are used by the channel adapters and the disk adapters and have control memories storing control information [Dunphy et al., figure 4, history log 404; column 9, lines 19-39; column 12, lines 55-68; column 13, lines 1-18; the cache memory in figure 2, 203 and figure 3, 305 also serve as part of the control memory]; and

Wherein the control information includes first control information and second control information [Dunphy et al., the corresponding first control information is associated with the serialization/deserialization of data, CRC/ECC generation, checking and correction and NRZ data encoding (column 10, lines 33-35), and the corresponding second control information is related to the generation of of M redundancy segments for error recovery purpose (column 11, lines 5-25)]

The first control information is stored in at least one of the control memories in each cluster, respectively, to be multiplexed across the clusters, and the first control information is management information which is used for controlling an operation of the disk array device [Dunphy et al., figure 2, 203], and

The second control information is stored in a separate control memory different from the said at least one of the control memories storing the first control information [Dunphy et al., figure 3, 305].

As to claim 3, Dunphy et al. and Belsan teach that **the second control information is storage structure information concerning a storage structure of the respective cache memories** [Belsan, a mapping table is easily maintained in memory of this data storage system to indicate which of the logical cylinders contained in the disk drive array (column 2, lines 8-38; figures 8-9). Note that the cache memory (figure 2, 113) contains the data to be transmitted to or received from the disk array, hence the mapping information reflects the storage structure of both the disk array and the cache memory].

8. *Related Prior Art*

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Fujimoto et al., (US Patent Application Publication 2004/0153691), "Fault Recovery Method and a Storage Controller in an Information Processing Apparatus."
- Okumoto et al., (US Patent Application Publication 2003/0204683), "Method, System, and Storage Controller for Controlling Shared Memories."
- Abe et al., (US 6,385,114), "Memory Package, Memory System and Hot-Line Insertion/removal Method Thereof."

- Cochran et al., (US Patent Application Publication 2005/0097132), "Hierarchical Storage System."
- Cochran et al., (US Patent Application Publication 2004/0267959), "Storage System with Link Selection Control."

Conclusion

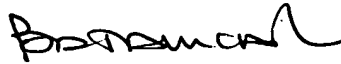
9. Claims 1-15 are rejected as explained above.
10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

August 15, 2005


PIERRE BATAILLE
PRIMARY EXAMINER
8/17/05